Available online at www.scholarsresearchlibrary.com

Scholars Research Library

Archives of Physics Research, 2011, 2 (4):34-37
(http://scholarsresearchlibrary.com/archive.html)

Scholars Research Library
ISSN : 0976-0970
CODEN (USA): APRRC7

Behaviour of CdS thin film transistors with Nd_2O_3 and La_2O_3 as GATE insulator

Muhidhar Puzari

Department of Physics, North Lakhimpur College, Lakhimpur, Assam, India

---

ABSTRACT

Nd_2O_3 and La_2O_3 have been used as gate insulator in CdS Thin-film Transistors(TFTs) fabricated in staggered electrode structure by multiple pump down (MPD) method of vacuum evaporation. The characteristics of the devices are presented and electrical parameters like trans conductance, output resistance, amplification factor and gain band-width product are evaluated. Suitable theoretical model is employed to estimate the trap density, critical donor density, grain size and mobility.

Key Words: Thin film transistor, rare earth oxide.

INTRODUCTION

The TFT is said to be tailor-made for display applications [1]. The choice of semiconductor-insulator combination plays a key role in determining it's ultimate properties [2]. A poor quality dielectric can increase the leakage current [3]. CdS is one of the first materials to be used in TFTs. Vacuum evaporated Nd_2O_3 films [4] having chemical and mechanical stability, high breakdown field strength (1.5×10^6 V cm^{-1}), low dissipation factor (~.0045) and high dielectric constant (12.64) fulfills the requirements of good insulators [4,5]. La_2O_3 is also recommended as good insulator for TFTs due to it's high capacitance density (0.15 F/cm^2), high dielectric constant (18), low loss (0.016) and high breakdown field strength (10^6 V/cm) [6].

MATERIALS AND METHODS

TFTs have been fabricated by MPD method on chemically and ultrasonically cleaned glass substrates by vacuum deposition of different layers in the given sequence: aluminium source drain electrode, CdS at elevated substrate temperature (200^oC), oxide layer and finally the aluminium gate electrode. Various geometrical patterns were obtained with the help of

mechanical masks. The channel was defined by a 50 μm wire grill fixed on the source drain mask. All the depositions were made in vacuum of the order of 10^{-6} torr. Film thickness was measured by multiple beam interference method. The fabricated samples were annealed in air at 200 ^{o}C for 3-4 hours and then stored in clean desiccator for 20-25 days to obtain stable and saturated characteristics.

RESULTS AND DISCUSSION

The drain current I_D vs drain voltage V_D characteristics for CdS- Nd_2O_3 and CdS- La_2O_3 TFTs are shown in figures 1and 2 respectively.

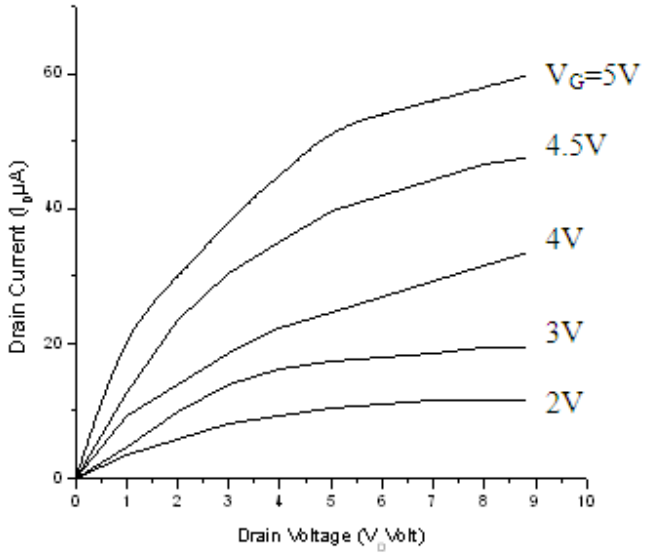

Figure1: Source- drain characteristics of CdS- La_2O_3 TFTs.

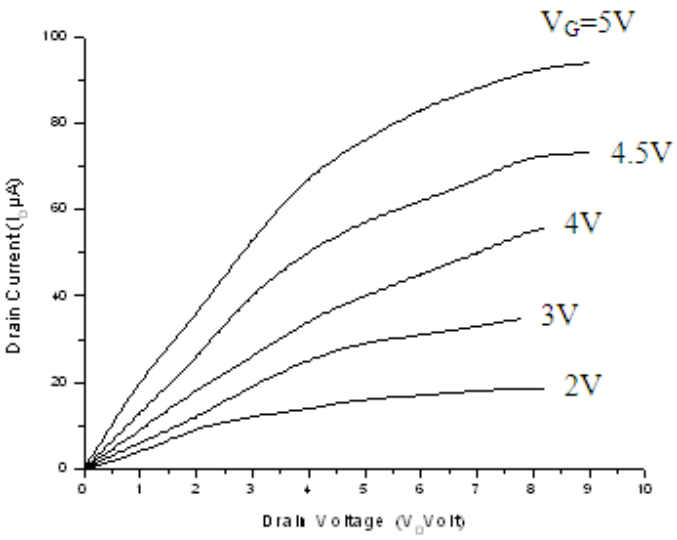

Figure2: Source- drain characteristics of CdS- Nd_2O_3 TFTs.

The field effect characteristics of CdS- Nd_2O_3TFTs (curve 'a' scale A) and CdS- La_2O_3 TFTs (curve 'b' scale B) at V_D = 8V are shown in figure 3. The pinch-off voltage for these two types of TFTs are -1V and -1.8 V respectively.

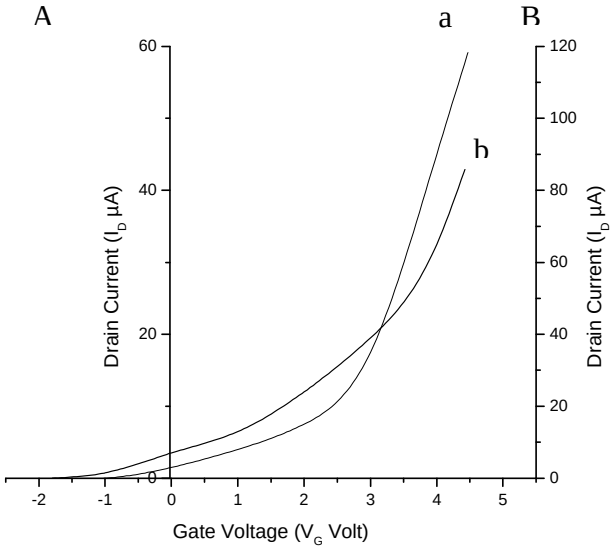

Figure3: Field effect characteristics of CdS- Nd_2O_3TFTs (curve 'a' scale A) and CdS- La_2O_3 TFTs (curve 'b' scale B)

Various transistor parameters like trans conductance (g_m), output resistance (r_d), amplification factor (µ) and gain band-width product as calculated from the characteristics are presented in Table 1.

Table 1.

Device type	Trans conductance g_m (µmho	Output resis-tance r_d (KOhm)	Amplification factor (µ)	Gain-bandwidth product (KHz)
CdS- Nd_2O_3	40	444	16.7	6.24
CdS- La_2O_3	55	333	18.3	7.55

Due to the polycrystalline nature of the CdS film existence of traps in the devices is most common. Hence the grain boundary trapping model [7] may be used to characterize the TFTs. According to this model the drain current I_D of a TFT with polycrystalline material is given by

$$I_D = w\mu_b (V_D/l) C_i V_G \exp (-q^3N_t^2t / 8\varepsilon KTC_i) \qquad (1)$$

Where w and l are the channel width and length, μ_b is the mobility, C_i is the insulator capacitance per unit area, N_t is the trap concentration per unit area and t is the thickness of the semiconductor film.

It is evident from equation (1) that the plot of *l*n (I_D/V_G) as a function of $1/V_G$ is a straight line from the slope of which N_t can be obtained. From the pre exponential part of equation (1) the value of mobility can be estimated.

The departure from linearity of this graph occurs when

$$N_G / t = N^*_D$$

Where $N_G = (C_i / q) V_G$ and N^*_D is the critical donor density. The crystal size L can be estimated from $N^*_D = N_t / L$. The value of different parameters obtained for the present devices are listed in Table 2.

Table 2.

Device type	Trap density N_t (x $10^{12}cm^{-2}$)	Critical donor Density N^*_D (x$10^{18}cm^{-3}$)	Grain size L (Å)	Mobility μ_b ($cm^2V^{-1}S^{-1}$)
CdS- Nd_2O_3	5.92	3.05	194	1.11
CdS- La_2O_3	4.74	2.59	183	0.66

The low value of mobility may be due to increased surface scattering for the introduction of surface states by atmospheric contamination during exposure of the semiconductor layer prior to the deposition of the oxide film [8]. A high interface trap density at the semiconductor dielectric interface can increase the threshold voltage restricting operation of the TFT at high voltage [9]. However, for some applications such as pixel select transistors a modest mobility of ~ 1 $cm^2V^{-1}S^{-1}$ is also adequate [10].

Periodic record of I-V data revealed that devices of both types deteriorated with time. Absorption of water vapour is perhaps the prime cause of device deterioration.

CONCLUSION

CdS- Nd_2O_3 and CdS- La_2O_3 TFTs exhibit good channel modulation. But they lack long term stability and have low mobility. Improved fabrication techniques might be needed to remove these discrepancies. The electrical parameters of Nd_2O_3 TFTs are slightly better and sensitivity of La_2O_3 towards humidity leads to it's faster deterioration.

REFERENCES

[1] T P Broady: *IEEE Trans. Electron Devices* 31, 1614 **1984**
[2] J C Anderson: *Thin Solid Films* 36, 299 **1976**
[3] G Bersular, P Zeitzoff and H R Huff: *Matter Today* 7, 26 **2004**
[4] V S Dharmadhikari and A Goswami: *Thin Solid Films* 87,199 **1982**
[5] A Van Calster and A D Voss: *Electrocomp.Sci.Technol.*6, 131 **1980**
[6] T Mahalingam, M Radhakrishnan and C Balasubramanium: *Thin Solid Films*, 78, 229, **1981**
[7] J Levinson, F R Shepherd, P J Scanlon, W D West Wood, G Este and M Rider: *J. Appl. Phys.*53(2) 1193 **1982**
[8] M Puzari and B Baishya : *Indian J. Phys.* 71A (3) 323 **1997**
[9] P F Carcia, R S Mcleon ,M H Reilly and G Nunes: *J. Appl. Phys. Lett.* 82, 1117 **2003**
[10] P F Carcia, R S Mcleon and M H Reilly: *Appl. Phys. Lett.* 88, 123509 **2006**