Available online at www.scholarsresearchlibrary.com

Scholars Research Library

Archives of Physics Research, 2011, 2 (4):45-49
(http://scholarsresearchlibrary.com/archive.html)

ISSN : 0976-0970
CODEN (USA): APRRC7

Effect of ambient atmosphere on the stability of $CdSe-La_2O_3$ thin film transistors

Muhidhar Puzari

Department of Physics, North Lakhimpur College, Lakhimpur, Assam, India

ABSTRACT

A rare earth oxide (La_2O_3) has been used as gate insulator in CdSe Thin-film Transistors (TFTs) fabricated in staggered electrode structure by multiple pump down (MPD) method of vacuum evaporation. The device parameters are evaluated from the characteristics and the effect of ambient atmosphere is investigated through periodic monitoring of data. It is observed that the device characteristics deteriorated with time and ambient exposure contributed to faster deterioration.

Key Words: Thin Film Transistor, device parameters, ambient effect.

INTRODUCTION

A thin-film transistor appears to be the most promising for an all thin film integrated circuit. The performance of an active device depends primarily on the physical properties of the materials used in it's fabrication [1]. A poor quality dielectric can increase the leakage current [2]. A rare earth oxide La_2O_3 is recommended as good insulator for TFTs due to it's high capacitance density (0.15 F/cm^2), high dielectric constant (18), low loss (0.016) and high breakdown field strength (10^6 V/cm) [3]. TFTs with a CdSe active layer have been used for the active addressing in flat-panel liquid crystal displays. They are also reported to be suitable for the high voltage addressing of light valves and electroluminescence displays [4]. But one of the failure mode of electronic circuits is the contribution of a layer of absorbed water vapour [5]. Stability, reliability and reproducibility are the prime requirements of an electronic device for widespread industrial applications. As such the stability of $CdSe-La_2O_3$ TFTs in ambient atmosphere is investigated and reported in this paper.

MATERIALS AND METHODS

TFTs have been fabricated by MPD method on chemically and ultrasonically cleaned glass substrates by vacuum deposition of different layers in the given sequence: aluminium source drain electrode, CdSe at elevated substrate temperature (200^0 C), oxide layer and finally the aluminium gate electrode. Various geometrical patterns were obtained with the help of mechanical masks. The channel was defined by a 50 μm wire grill fixed on the source drain mask. All the depositions were made in vacuum of the order of 10^{-6} torr. Film thickness was measured by multiple beam interference method. The fabricated samples were annealed in air at 200 °C for 3-4 hours and then stored in clean desiccators for 20-25 days to obtain stable and saturated characteristics. To assess the impact of ambient atmosphere the stability of the devices I-V data was recorded at different periods of time. Thereafter the samples were left in ambient atmosphere and I-V data was noted till the TFTs collapsed. Some important transistor parameters like trans conductance and mobility are also evaluated from time to time.

RESULTS AND DISCUSSION

The source-drain characteristics of a fresh sample of CdSe-La_2O_3 TFT at different gate voltages (V_G) are shown in figure 1. Figure 2 shows the characteristics of the fresh sample (curve 'a'), after 30 days (curve 'b') and 60 days (curve 'c') in clean desiccators. While the curves 'd' and 'e' are the characteristics of the sample in ambient atmosphere after 15 days and 30 days respectively at V_G = 5V.

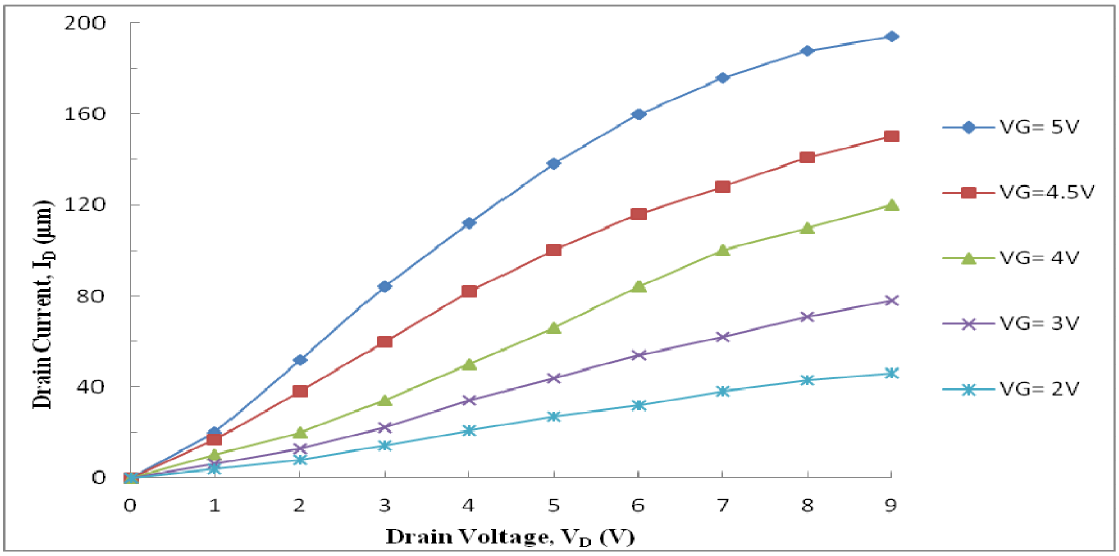

Figure1: Source-drain characteristics of a fresh sample of CdSe- La_2O_3 TFT.

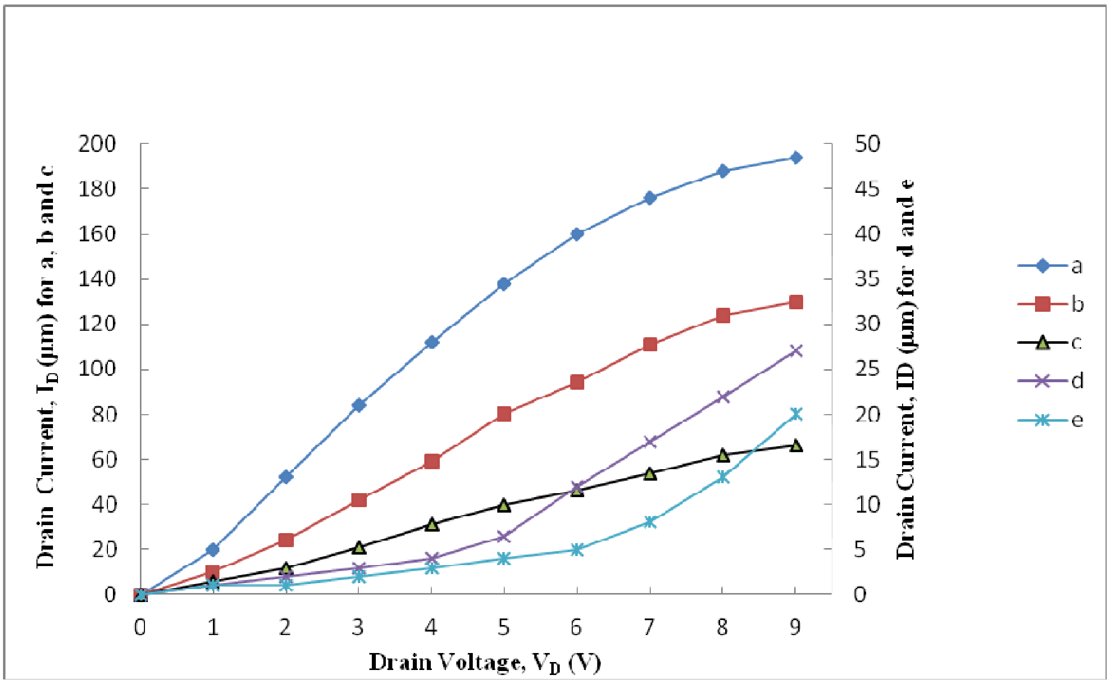

Figure2: Source- drain characteristics of CdSe- La_2O_3 TFT at different periods of time.

During the period of investigation the value of trans conductance and mobility decreased appreciably as presented in table 1.

Table 1

Device type	Device parameter	Fresh sample	After 1 month	After 2 months	Ambient exposure of 15 days
CdSe- La_2O_3	g_m (μmho	120	80	50	4
	$\mu_b(cm^2V^{-1}S^{-2})$	0.61	0.45	0.32	0.03

Thus it is apparent that the device characteristics deteriorate with time and the ambient exposure accelerates the process of deterioration. The pinch-off voltage was also found to decrease by 0.6V. According to Weimer [6] the presence of donor like states at the interface is responsible for the increased negative value of pinch-off voltage. A high density of donor like states at the interface bends the bands down and provides an accumulation layer at zero gate bias. A negative gate voltage is required to pinch off this current. Thus the increased negative value of pinch-off voltage is an indication of increasing donor like surface states with time.

Van calster and De Vos [7] have pointed out the following two drift phenomena responsible for low frequency instability of the TFTs.

(i) Mobile ions in the insulator film which cause a delayed gain of the field effect.
(ii) Slow states at the S-I interface, which cause a delayed attenuation of the field effect.

A high interface trap density at the semiconductor dielectric interface can increase the threshold voltage restricting operation of the TFT at high voltage [8]. The value of mobility of the fabricated devices is also quite low. It might be due to increased surface scattering for the introduction of surface states by atmospheric contamination during exposure of the semiconductor layer prior to the deposition of the oxide film [9]. However, for some applications such as pixel select transistors a modest mobility of ~ 1 $cm^2V^{-1}S^{-1}$ is also adequate [10].

A number of factors are thought to be responsible for device deterioration and collapsing. The oxide used in this investigation though claimed to be 99.9% pure by the manufacturer, may be contaminated with ions which move through the film under the influence of applied electric field. The glass substrates may also contribute towards instability though they are cleaned carefully. In the MPD method of TFT fabrication a layer of air and other atmospheric contaminants might remain trapped in between the semiconductor and the insulator layer. Such a trapped layer might contain sufficient moisture which would help oxidation of the CdSe film and contribute towards the fast states. During ambient exposure of the semiconductor film foreign contaminants both neutral and ionized may also enter the S-I interface. Some contaminants or a layer of air might also be trapped in between the glass substrate and the dielectric film. An absorbed layer may represent a channel both for ion migration and electron migration[11]. During the period of stability investigation these impurities might have slightly diffused in to the CdSe layer to increase the surface states.

Another influencing factor affecting the TFT performance is the nature of s-d contacts. For achieving ideal characteristics the contacts between s-d electrodes and semiconductor film should be ohmic. Though aluminium is known to make a satisfactory ohmic contact with CdSe film, due to ambient exposure of the s-d electrodes prior to the deposition of the CdSe film, a thin insulating barrier air or other contaminants might remain trapped between these two films. Such a barrier would degrade the contact between s-d electrodes and CdSe film. Again the scattering of Al to the s-d gap during electrode deposition would also introduce acceptor like states in the semiconductor film [6]. Oxidation of Al electrodes with time is also responsible for degradation of s-d contacts [12].

CONCLUSION

TFTs fabricated by the MPD method with the semiconductor-insulator combination of CdSe and La_2O_3 do not exhibit long term stability. Ambient exposure further deteriorates its characteristics. Introduction of surface states and absorption of atmospheric vapour are the prime causes of device deterioration. Improved fabrication technique and suitable encapsulation might be needed to obtain stable characteristics.

REFERENCES

[1] M K Rao and S R Jawalekar, *Int J Electronics*, **1979**, 46, 3, 309-311.
[2] G Bersular, P Zeitzoff and H R Huff, *Matter Today*, **2004**7, 26.
[3] T Mahalingam, M Radhakrishnan and C Balasubramanium, *Thin Solid Films*, **1981,** 78, 229.
[4] G Moersch, P Rava, F Schwarz and A Paccagnelia, *IEEE Trans. Electron Devices*, **1989**, 36, 2, 449.
[5].G F Cerofolini and C Rovere, *Thin Solid Films*, **1977**, 47, 83.
[6] P K Weimer, *Physics of Thin Films*, **1964**, 2, 147.

[7] A Van Calster and A D Vos, *Electrocomp Sci Technol*, **1980**, 6, 131.
[8] P F Carcia, R S Mcleon ,M H Reilly and G Nunes, *J Appl Phys Lett*, **2003**, 82, 1117.
[9] P Singh and B Baishya, *Thin Solid Films*, **1987**, 147, 25.
[10] P F Carcia, R S Mcleon and M H Reilly, *Appl Phys Lett*, **2006**, 88, 123509.
[11] G F Cerofolini and C Rovere, *Thin Solid Films*, **1977**, 47, 83.
[12 I Blech, H Sello and L V Gregor, *Hand Book of Thin Film Technology*, Mc Graw –Hill, New York, **1970**.