

Effects of mask material conductivity on lateral undercut etching in silicon nano-pillar etching

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Abstract:

High aspect ratio silicon structures have gained significant interest due to its vast applications. Minimal lateral etch under the mask is essential to achieve very high aspect ratio silicon nanostructures. Previously, we reported that chromium oxide is better than metallic chromium as a hard mask for silicon etching in terms of etch rate and selectivity to resist during mask structure fabriction1. Here we report that insulating metal oxide etch mask like chromium oxide also provides less lateral etch than conducting metal etch mask using non-switch "pseudo-Bosch" dry etching. The mask structure was fabricated by electron beam lithography and liftoff, with all the metal and metal oxide coated by evaporation. Silicon was etched using a non-switching pseudo-Bosch process (Oxford Instrument Plasmalab100, 10 mTorr, 20 W RF power, 1200 W ICP power, 38 sccm C4F8, 22 sccm SF6, 15 o C, etches Si 390 nm/min)2.

Biography:

Ripon Dey has completed his PhD from University of Waterloo in Electrical Engineering and Postdoctoral Studies from School of Engineering, University of Waterloo (UW), Canada. He is the Research Scientist of Waterloo Institute for Nanotechnology (WIN), a premier Nanotechnology Engineering Research Institute in the globe. He has published more than 32 papers in reputed peer reviewed journals including 3 issued patents (Intellectual property) and has been serving as a senior reviewer of Elsevier Engineering. He is also Mitacs Research fellow in UW. Dr. Dey's research is focused on MEMS/NEMS Engineering, Nano-electronics, Material Engineering, Nano-sensor, nano- and microstructure fabrication.



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