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Investigation of Epitaxial Growth in Performance of MOS Devices

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ABSTRACT

The role of an epitaxial growth technique in the performance of metal oxide semiconductor (MOS) devices was investigated. Using a pioneering method like selective epitaxy, the performance and integration of MOS devices found to be improved significantly. It is also seen that epitaxy is essential for realizing modern semiconductor device like FinFETs. The cheap and improved semiconductor structure like vertical MOSFET also required service of epitaxy technique. The stringent control of the epitaxial process was necessary for achieving the superlative performance and desiredstructures.

Keywords: Epitaxy, MOSFET, MOS, FinFET

INTRODUCTION

We are living in an era where pretty much everything has something to do with electronic devices. The pillar of strength of any electronic industry is semiconductor devices. We already know that according to Gordon E Moore, the number of transistors per integrated circuits may double in every 18 months. He predicted this way back in 1965 and it's merely not a prediction now but a fact. The ever shrinking minimum length requirement brought four major enhancements (i) Higher speed (ii) lower power (iii) higher density and (iv) low cost. The world now becomes hungry for more performance and integration. In fact that is the driving force for the ever increasing research interest among scientist. This hungry brought us more well performing devices and significantly with low cost. This accelerated electronic industry.

The addition of VMOSFET which is fabricated mainly by epitaxy at first they outclassed BJTs in many aspects and making the design of amplifiers much cheaper and easier.

One of the latest trends in mos devices fabrication is the selective epitaxial growth of Si and SiGe at the recessed source and drain region which reportedly enhanced the performance of MOSFETs. This is especially crucial for modern MOS device like FinFET. Novel device structures, stalked structures can be realized by the selective epitaxial growth of Si and SiGe. The unique features of selective epitaxy need to understand well in order to make best out it for MOSFET applications.

Selective epitaxial growth of Si and SiGe in S/D region of MOSFET

The selective epitaxial growth has been implemented to study the variation in the MOSFET characteristics. This was intended to achieve an ultra-shallow junction as an elevated source and drain structure [1]. The elevated S/D structure induced stress in the channel region; the e-SiGe was successfully implemented to Pmosfet [2]. The performance of the MOSFET drastically increased as the stress in the channel region forced the holes for higher mobility.

Stringent control required for the selective epitaxy of SiGe in order to achieve the best performance with this e-SiGe structure. The shape of recessed region also plays an important role in the performance of MOSFET. The TEM image of the pMOSFET is shown in Figure 1 [3,4].

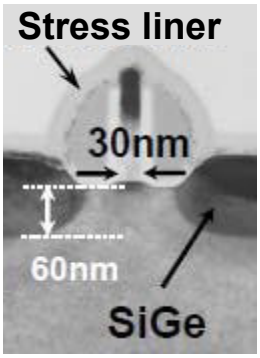

Figure 1: Cross-sectional TEM image of PMOSFET for which e-SiGe is applied

Two step recessed SiGe-S/D structure

The series resistance should be decreased along with the increase in channel stress without disturbing short channel effect (SCE). The effective way to reduce the series resistance has been found to be proximity control using boron doped (in situ) SiGe. Figure 2 shows three kinds of e-SiGe structures. But it should be noted that two step recesses is the only structure which can actually prevail over trade off SCE (Vth roll off) along with increasing stress.

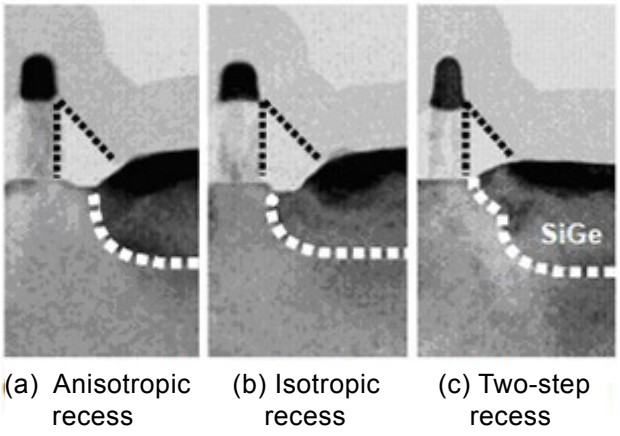

Figure 2: Three kinds of e-SiGe structures.

To control the SiGe growth precisely, the understanding of two dimensional growths is necessary. Generally, the rate of deposition is different for different crystal plane. It has been found that 110 oriented growth which is vital for hybrid oriented technique (HOT), helped to achieve desired structure [5,6]. Figure 3 shows typical structure of two step recessed source and drain. The major features are (i) optimizing source and drain recessed shape and SDE to increase the stress in channel region, (ii) optimization of halo profile and SDE recessed shape to control short channel effect, (iii) In situ doping and reduction of parasitic resistance [7].

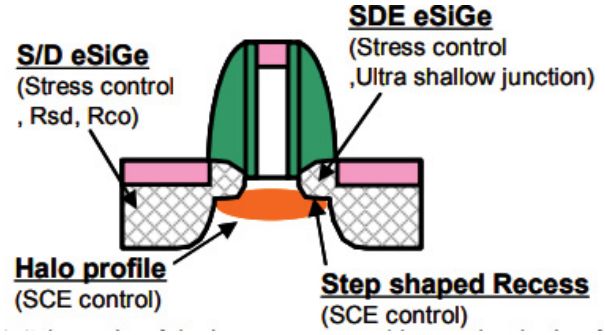

Figure 3: Schematic of two step recessed structure of S/D.

A simulation was carried out to study the impact of the structure on the stress [8]. Figure 4 shown the two steps recessed SiGe-S/D structure with fixed the depth of deep S/D to 60 nm.

Figure 4 indicates that the stress was increased when the gate length (Lg) is small and that the extension depth, with which the optimum stress is achieved, decreased with the gate length.

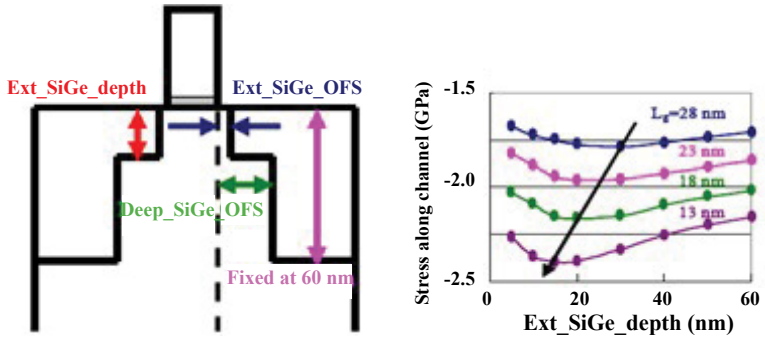

Figure 4: Two-step SiGe-S/D structure (left), stress vs depth simulation (right).

This result indicates that shallower SiGe depth is preferable for short gate length MOSFETs. Hence we can say that two steps recessed SiGe S/D structure is most significant method for inducing the stress in the channel region and thus increasing the device performance of pMOSFET [9,10].

Selective Epitaxy of FinFETs

Selective epitaxy plays a crucial role in realizing modern device like FinFETs for their improved performance as well as device operation as the Si body is so slight that the source and drain is resistance is certainly so high. However, the selective epitaxial growth with respect to FinFETs as compared to ordinary MOSFETs is much difficult.

This is because; there are certain requirement like pre bake step which executed under H_2 ambient in order to eliminate surface oxygen contamination.

Note that there are chances of surface Si atom being migrated and results in deformation of device shape. The thin thickness of Si layer (as thin as Lg) made the transformation of Si atoms most critical in FinFETs.

The epitaxial growth development also faces some difficulty. The region where Si should be grown is actually very small. The volume of the grown layer was constrained by the facet, which formed at the edge of selective epilayer. Here solid phase epitaxy was used for the selective epitaxy of FinFETs [11]. Here we are describing two important processing steps for the selective epitaxy of FinFETs.

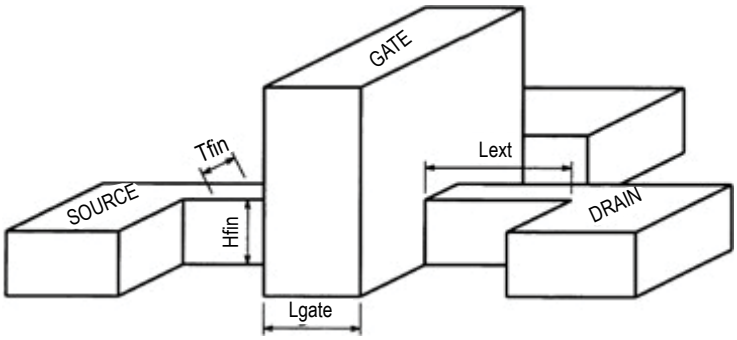

Figure 5: Schematic diagram of a FinFET.

Pre bake optimization

This step is critical in eliminating surface contaminants like oxygen. PBO requires UHV condition or H_2 ambient. An ideal blend of high temperature and low pressure will enhance the deoxidization for the precise case of Si with flat surface. However, for thin devices with thin Si layer, stringent control requires as the migration of surface Si atoms could result in the deformation of device structure in order to reduce the surface area.

The H_2 annealing can be used in a controlled manner to get rid of surface contaminants even without disturbing the device structure. The studies show that H_2 annealing at a temperature of 900°C and 380 Torr. The elevated S/D structure on FinFET was successfully realized with right H_2 annealing and device structure [12].

Solid phase epitaxy for FinFETs

Solid phase epitaxy and appropriate etching can be used in order to improve the Si region along with the suppression of random nucleation. The low temperature requirement (600 to 650) is much desired for small size FinFETs.

The single crystal growth of Si by SPE required only 6500 subsequently unwanted region selectively etched by using HCL. The low temperature requirement helps to avoid the agglomeration of Fin structures. Facet formation also can be avoided due to the Si edge control by the annealing temperature and timing of SPE [11,13].

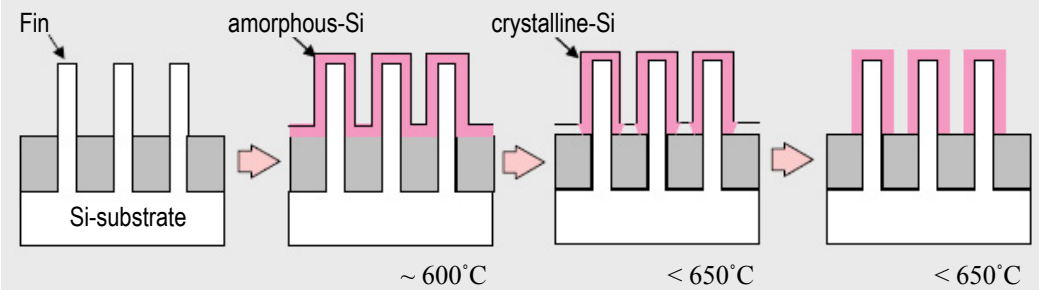

Figure6: Schematic diagram of SPE[15][13]

FinFETs exhibits low leakage, better sub threshold slope and better voltage gain. These are the main advantage of FinFETs over MOSFETs [14].

Vertical MOSFET (VMOSFET) is a modified version of planar MOSFET and which can be fabricated by Molecular Beam Epitaxy. The device was realized almost whole fully through epitaxy [15].

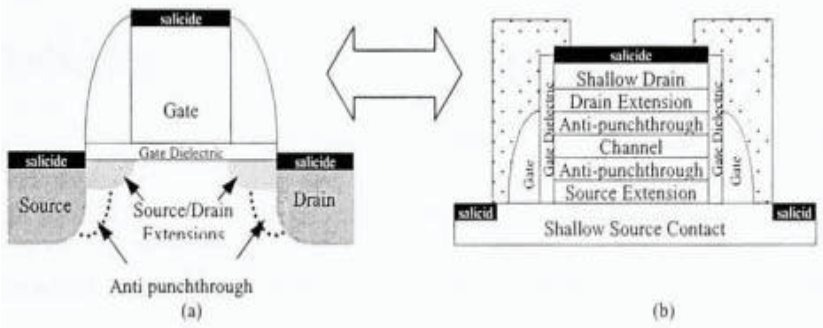

Figure 7: Planar mosfet*vs*vmosfet

The most expensive process in the fabrication of any semiconductor device is lithography. But in the case of VMOSFET lithography was not required as the channel length was not defined by lithography. This reduced expenses significantly.

The distance between source and drain gets reduced and this will increase the speed of the device as the time taken for a carrier to cover this distance gets reduced.

The VMOSFETs are composed of both front gate and back gate. This multiple gate alignment made a huge impact in enhancing the device density.

CONCLUSION

We have seen that techniques such as selective epitaxy play an important role in improving the performance of MOS devices significantly. The selective epitaxial growth has been implemented to achieve an ultra-shallow junction as

an elevated source and drain structure. The elevated S/D structure induced stress in the channel region which forced the holes for higher mobility and hence increased device performance.

We also have seen that epitaxy is an essential requirement for realizing modern MOS devices like FinFET. The facet formation and agglomeration of fin structures was successfully controlled by the solid phase epitaxy as the process required a low temperature condition. But the stringent control is necessary for achieving high quality devices.

The epitaxially grown VMOSFET was significantly brought down the expenses for the fabrication as the process carried out without lithography, the most expensive part of any device fabrication. The reduced source and drain distance enhanced the device speed. The multiple gate alignment enhanced the density of the device and power consumption also got scaled down.

The ever advancing epitaxy technique is definitely going to boost semiconductor industry further.

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